"This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 644080."

SAFURE

SAFety and secURity by dEsign for interconnected mixed-critical cyber-physical systems

METrICS: a Measurement Environment for Time Critical Systems

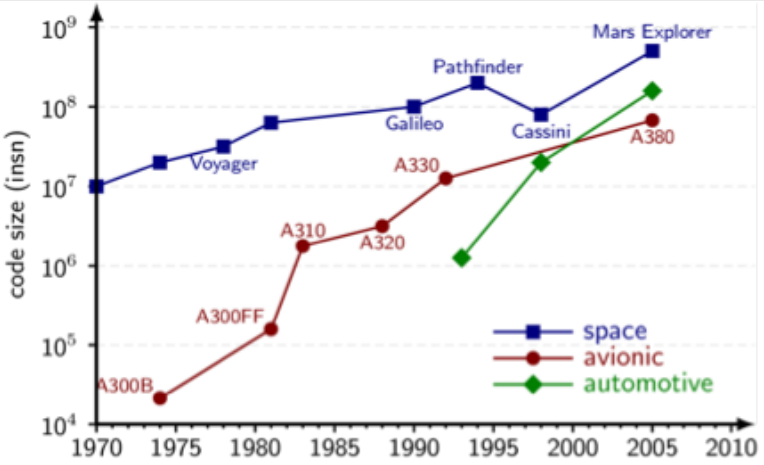
Sylvain Girbal, Thales Research & Technology

HiPEAC 18, Manchester, 22nd-24th January 2018

Safety-Critical & Time-Critical Context

Performance Requirements

- Exponential increase of performance requirements
- Unsustainable with classical single-core embedded solutions
- Multi-core architectures ➔ promising candidate with regards to Size, Weight and Power (SWaP)
- Multi-core are oriented toward the consumer electronic market



Compliance with regulation standards ➔ Certification

- **Spatial partitioning**: No application or task should be able to access / **alter** the **data** of another application or task.
- **Time partitioning**: No application or task should be able to **delay** another application or task.

How to ensure a sufficient level of **time determinism** with multi-core COTS architectures?

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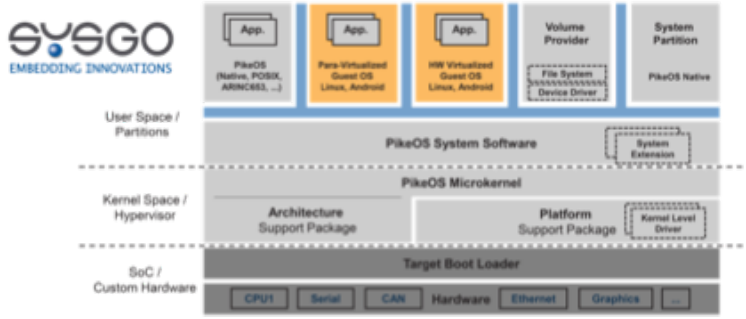
Target Architecture & Environment

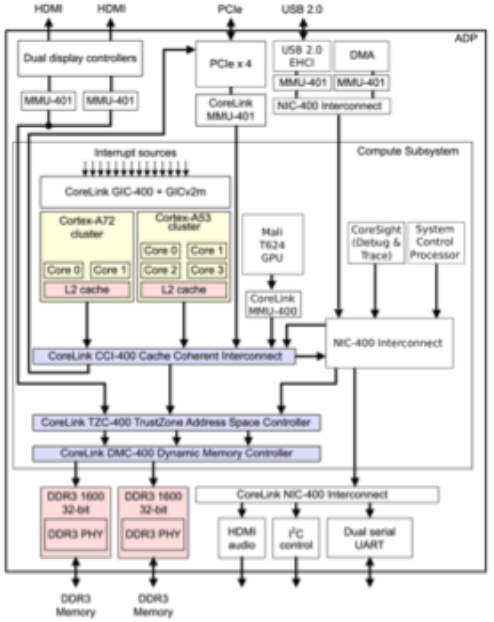
PikeOS RTOS from SYSGO AG

- Real-Time Operating System
- Separation Micro-Kernel
- Partitioned Environment
- Virtualization



ARM Juno BOARD

- A hi-performance bi-core out-of-order ARM-v8 Cortex A72 core cluster
- A more predictive quad-core in-order ARM-v8 Cortex A53 core cluster
- Multi-core COTS not specifically designed for real time systems with a large set of **shared hardware resources**



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OPEN

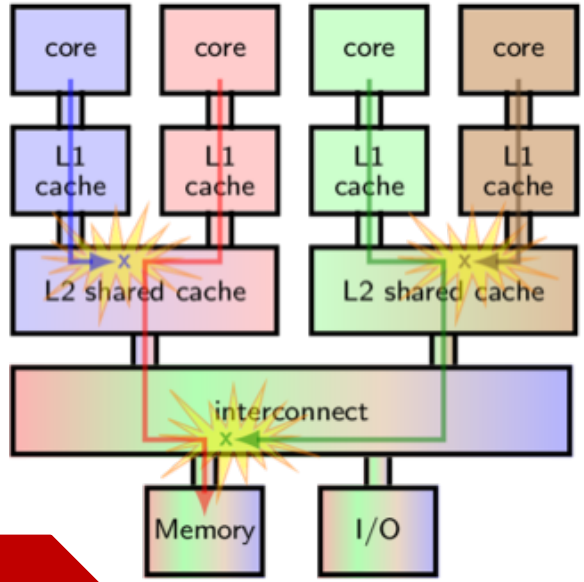
The Challenge of Timing Interferences

Using multi-core COTS in Safety Critical Systems

- Successfully faces the exponential increase of performance requirements
- But focuses on **best-effort** performance, not on **worst-case** performance

The problem: inter-core timing interferences

- Multi-core ➔ shared hardware resources
- Concurrent accesses to these resources are involving some **arbitration mechanisms** at hardware level
- Hardware contention is introducing unpredictable **timing interference** appearing as extra time delays
- Breaking the **time isolation** principles



How to measure **timing interferences** in real systems?
Can we **correlate** with **hardware resource** accesses?

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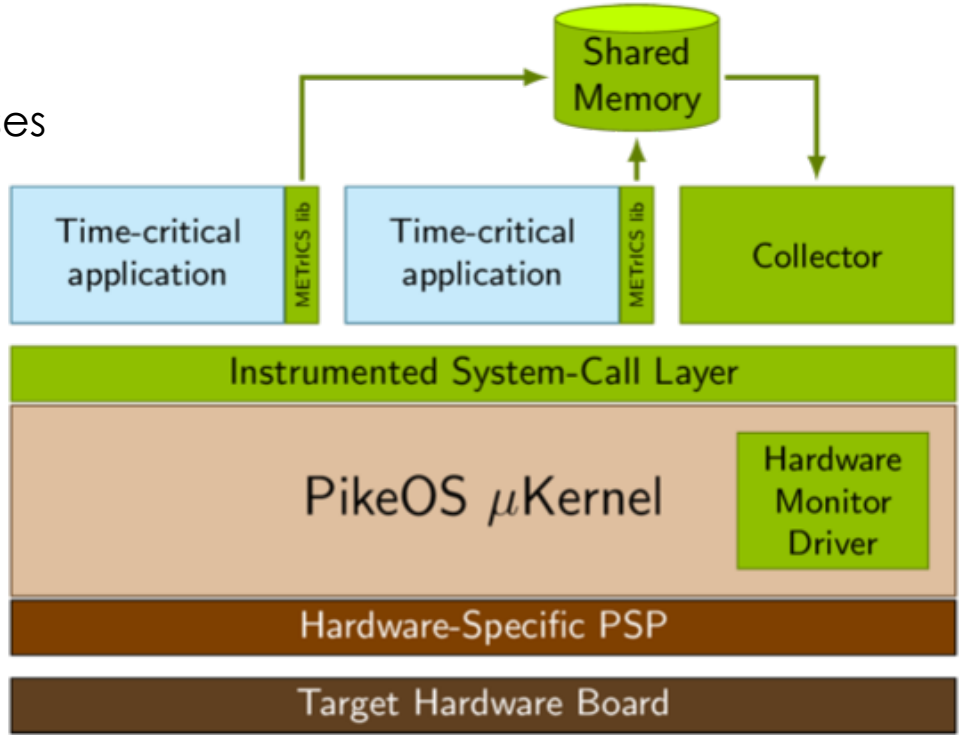
METrICS: a Measurement Environment for Time Critical Systems

Features

- Running on top of the PikeOS RTOS
- Providing accurate measurement of timing and hardware resource accesses
- Rely on hardware time base & performance monitor counters
- Minimizing timing intrusiveness
- Ability to observe timing interference

Software Architecture

- Driver
- Library
- Collector
- SHM
- Instrumented Syscalls



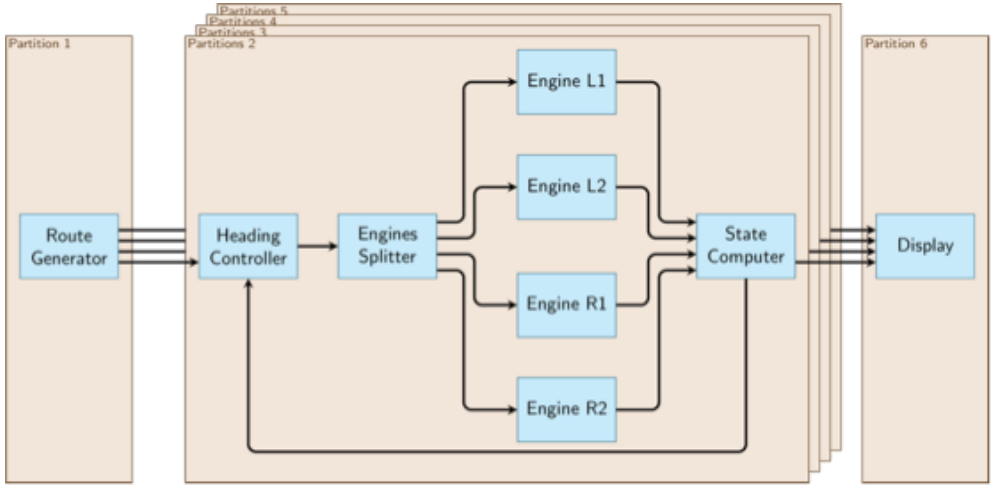
Driving Example: Drone Swarm Application

Description

- Control-command application guiding a set of 4 quadri-copters along a pre-set track

Software Architecture

- Route Generator
- Drone Control (x4)
  - Kinematic model of a drone
  - Controlling velocity and heading
  - Dynamic model controlling DC motors
- Display



How is this particular deployment sensitive to **timing interferences**?

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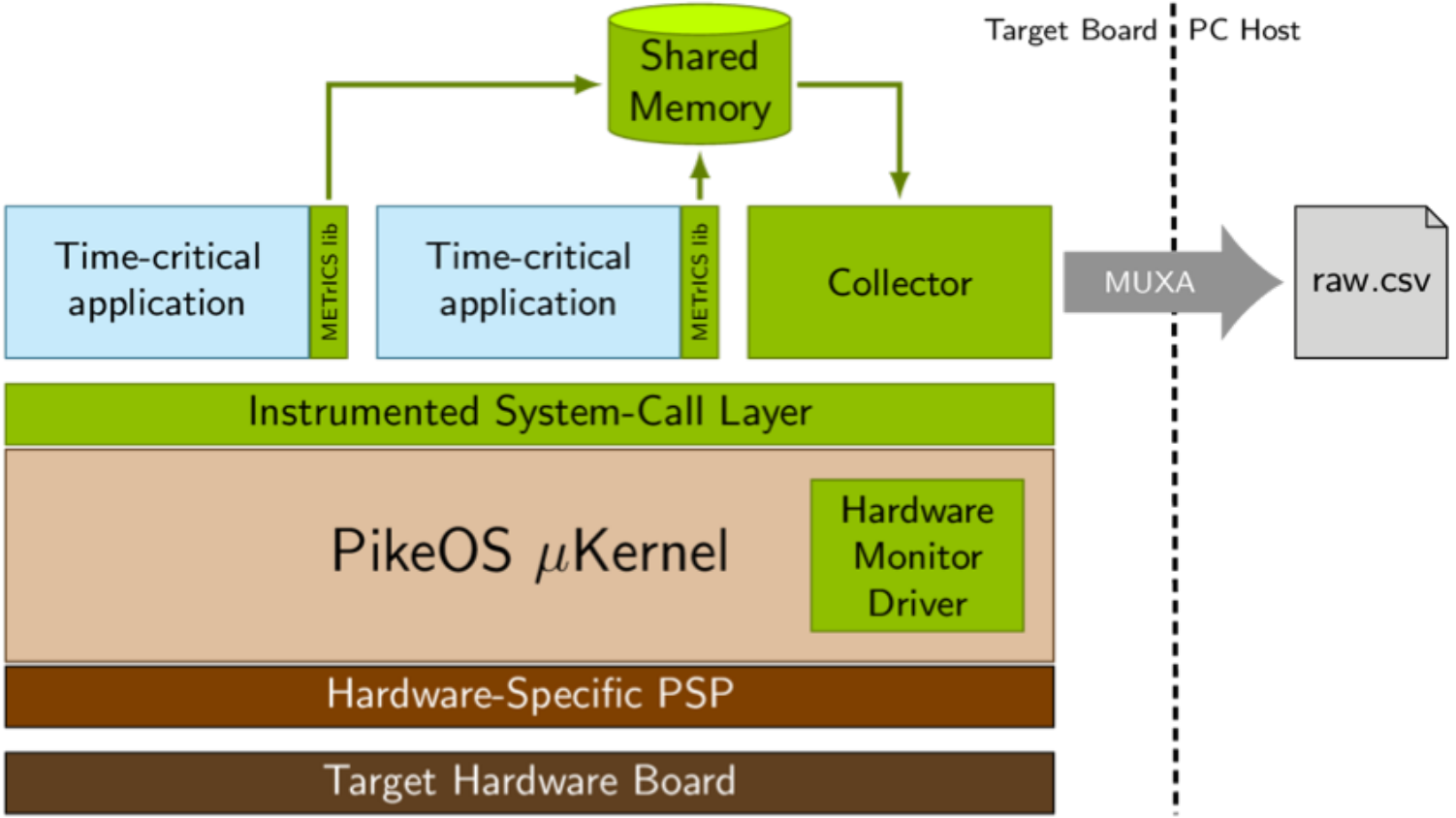
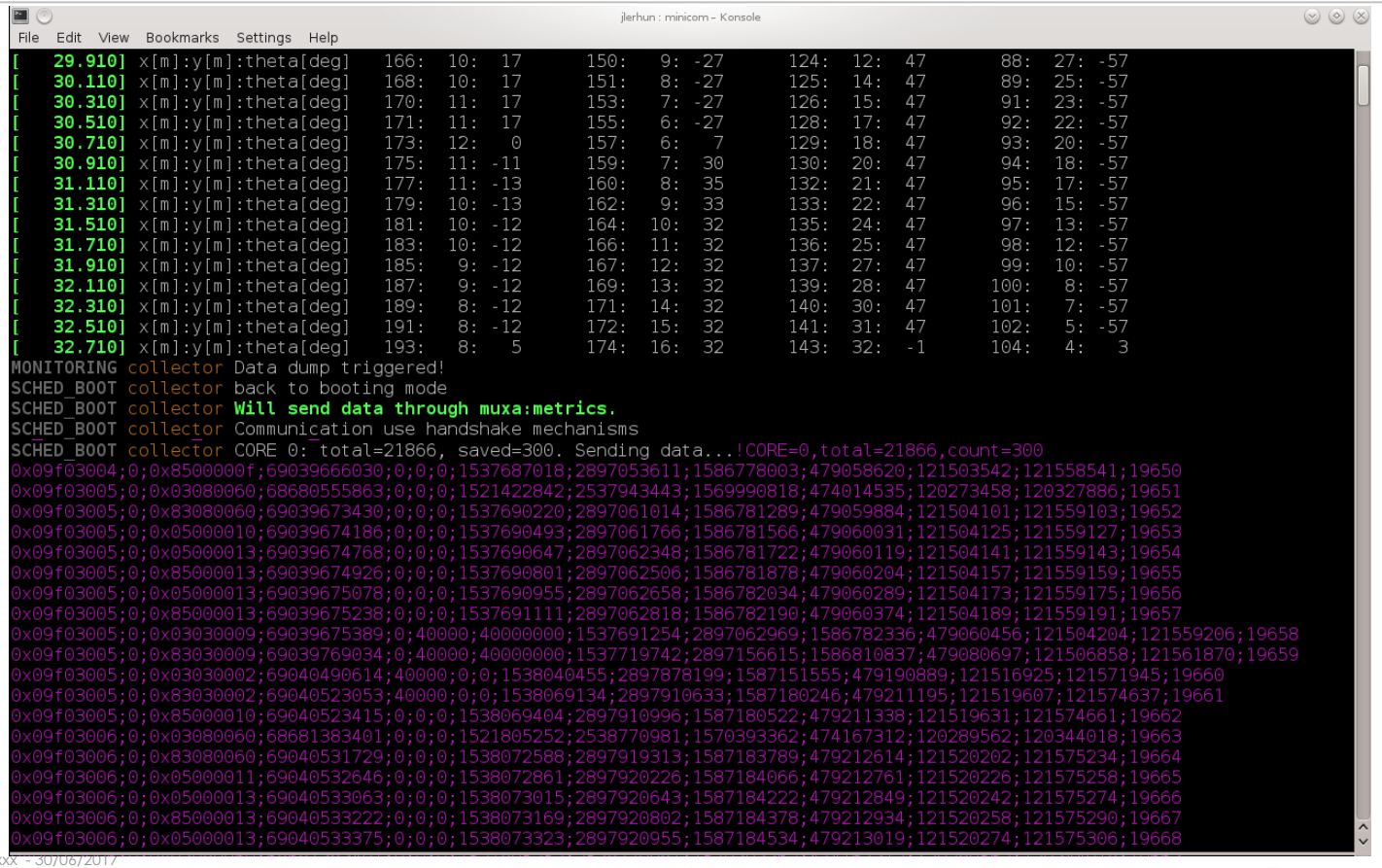
Collecting raw performance data with METrICS



Collecting raw performance data with METrICS



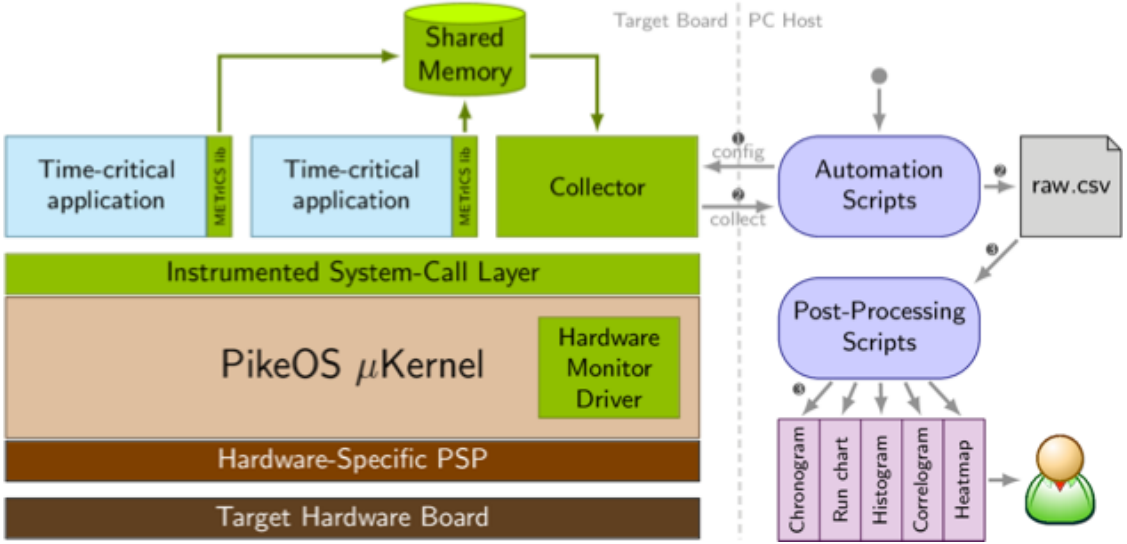
Configurations & METrICS Automation

Application deployments	4
Single-core, AMP, SMP, Hybrid	
Buffer size	3
Fitting in L1, Fitting in L2, Not Fitting	
Cache Policies	2
Flushing / Not Flushing between time partitions	
Hardware Counter Selection	
6 selected among 41 pre-selected	C_{41}^{6}
Number of runs	1000
For statistical significance	
TOTAL RUNS	**108 Billion**

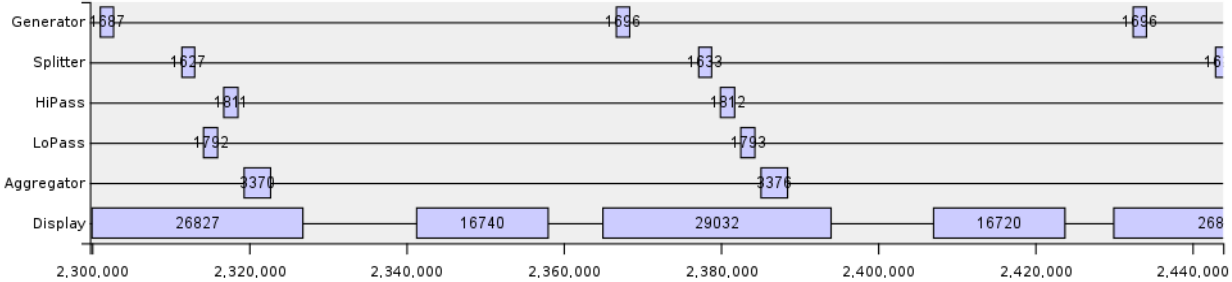
➔ Need to **reduce** the **Design Space**
➔ **Automation** necessary

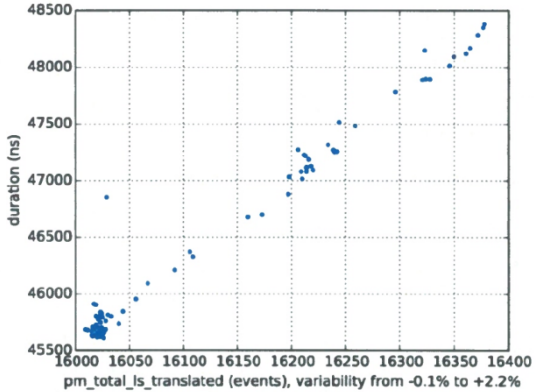
Studying correlation between counters

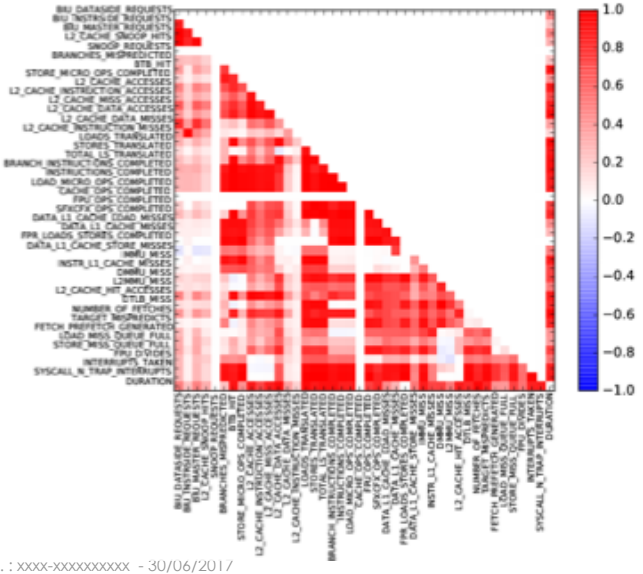
- More than 100GB of raw data
- Around 14 days of runtime

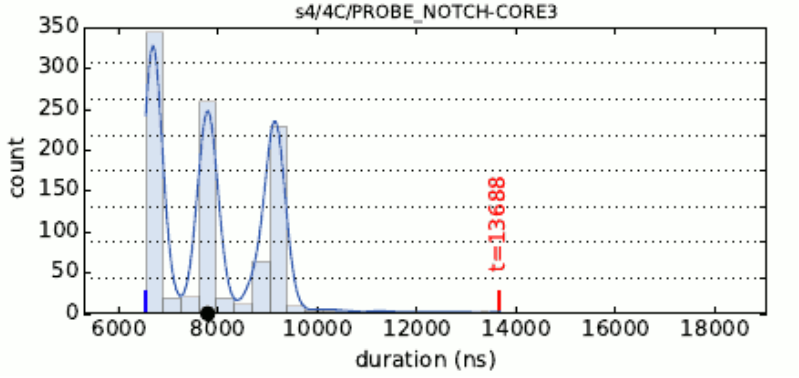


Rendering performance data collected with METrICS

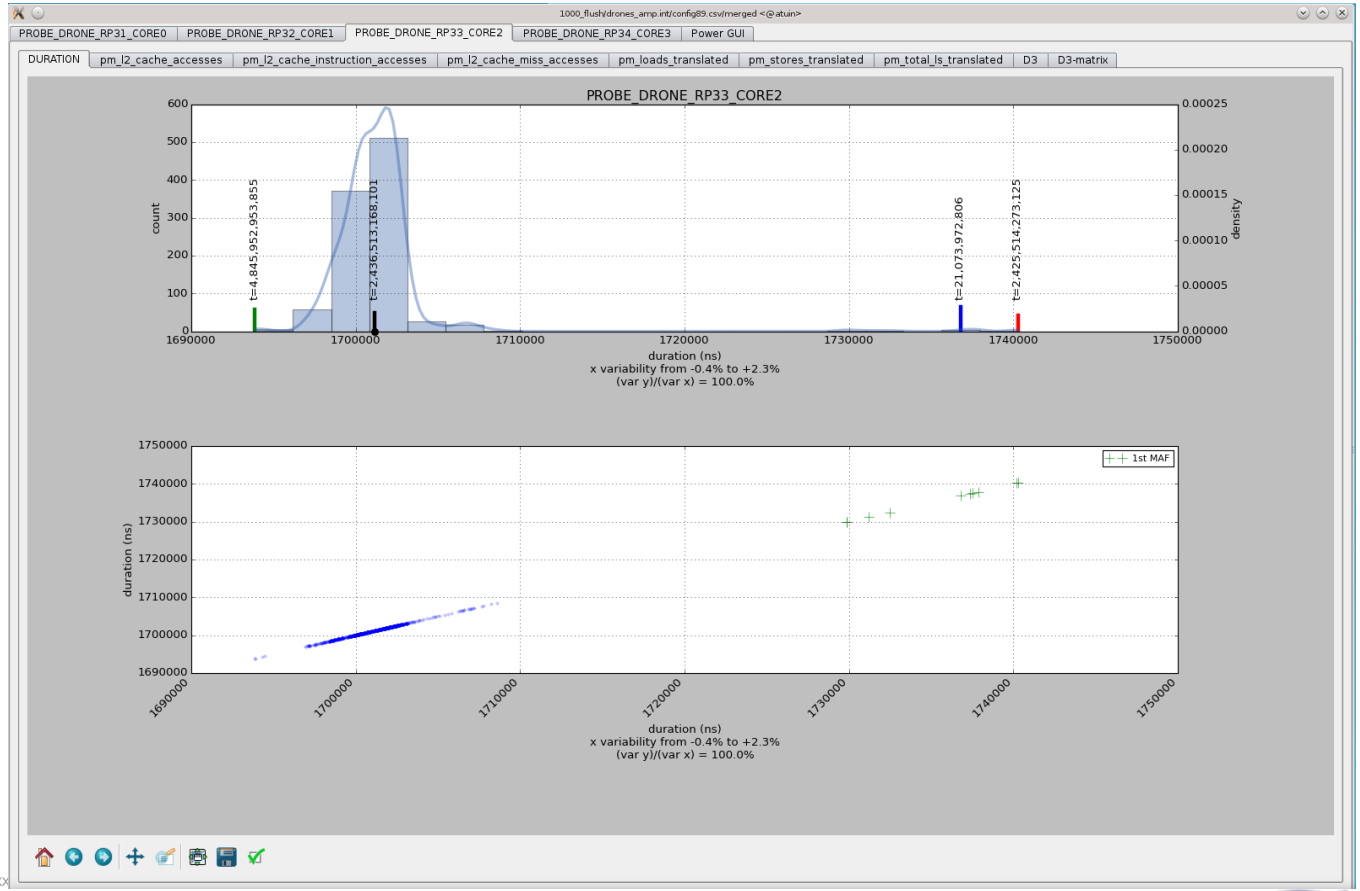




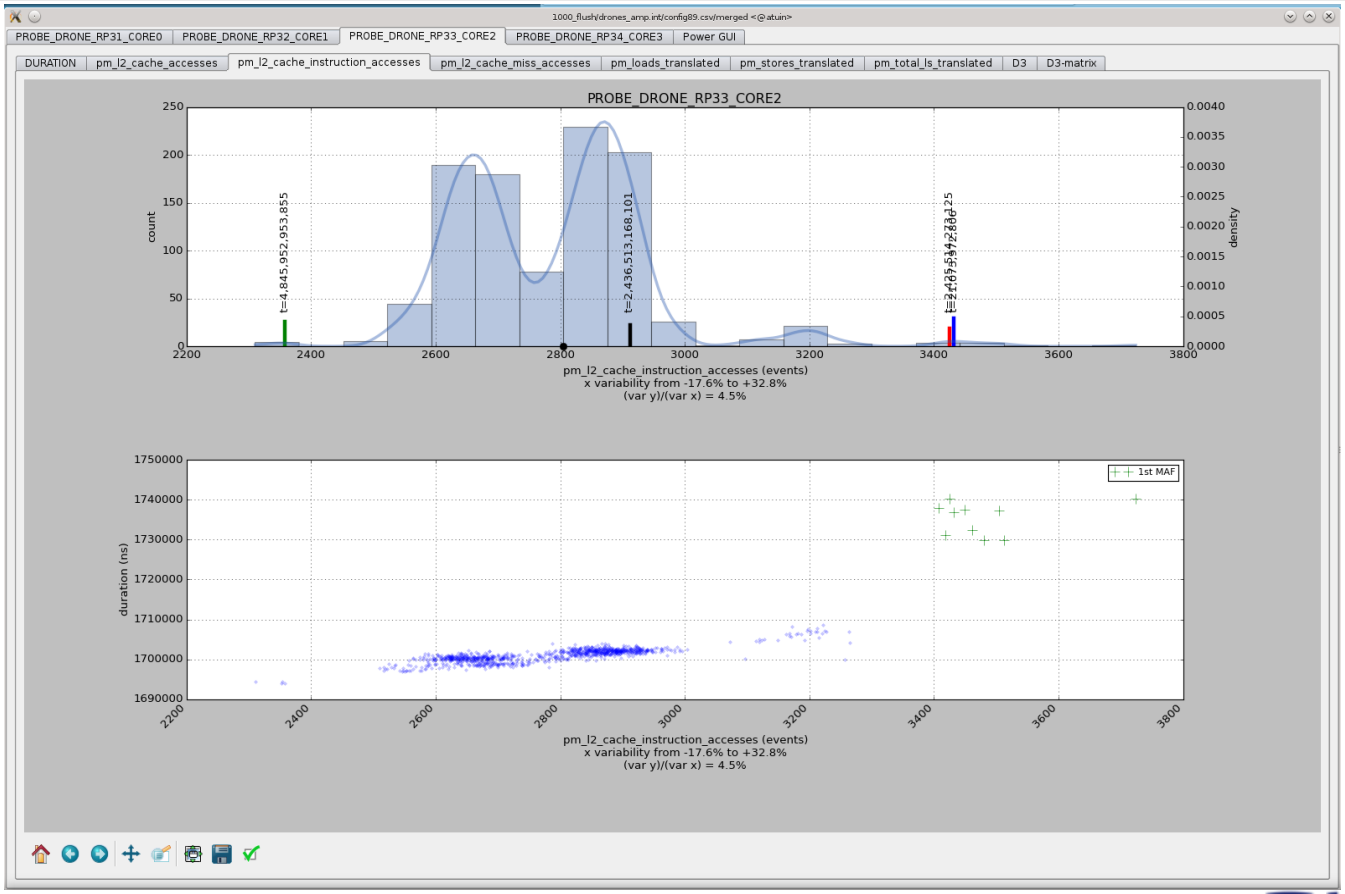




Timing Histograms



Resource access histograms & Timing VS access correlograms



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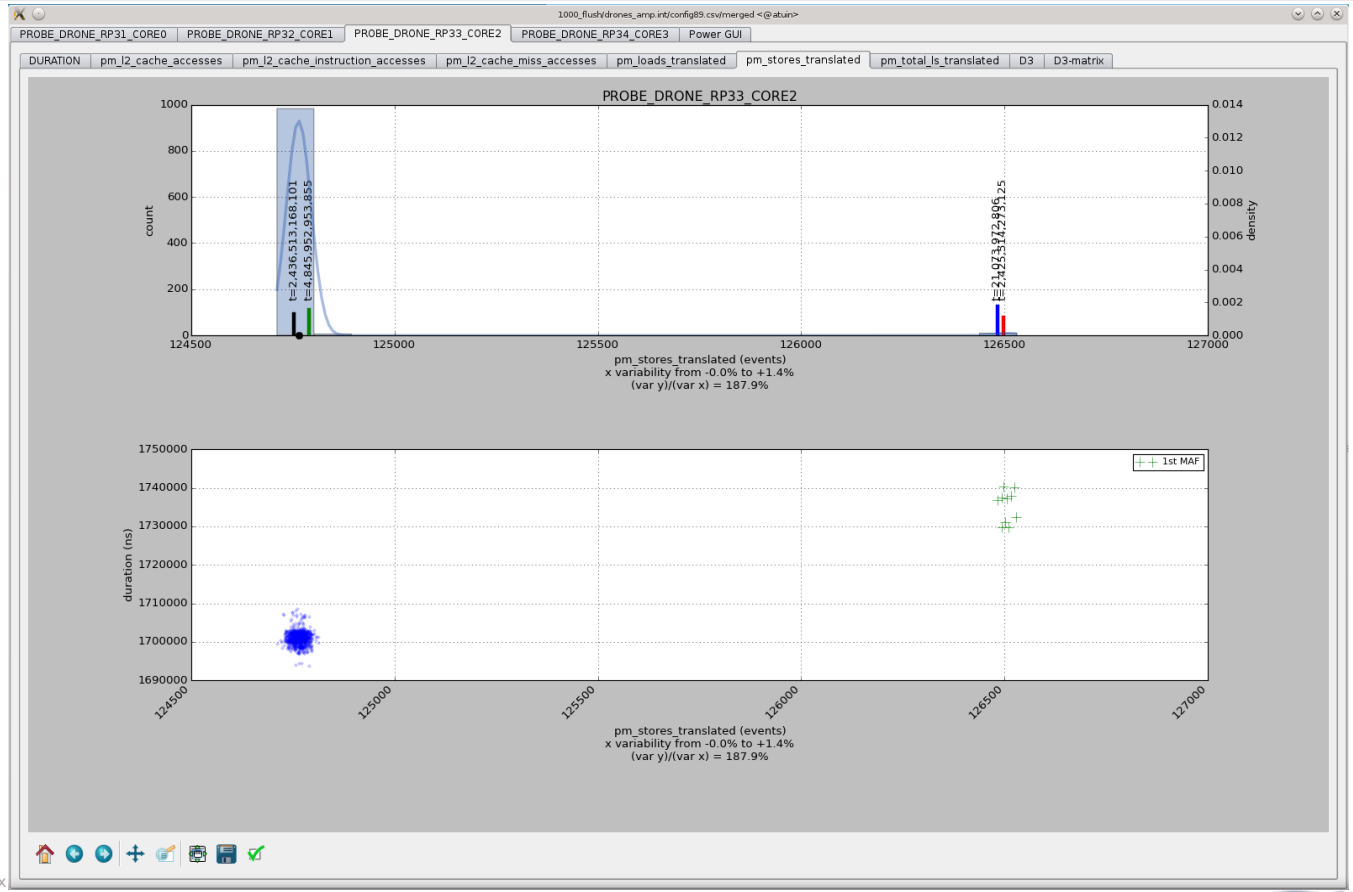
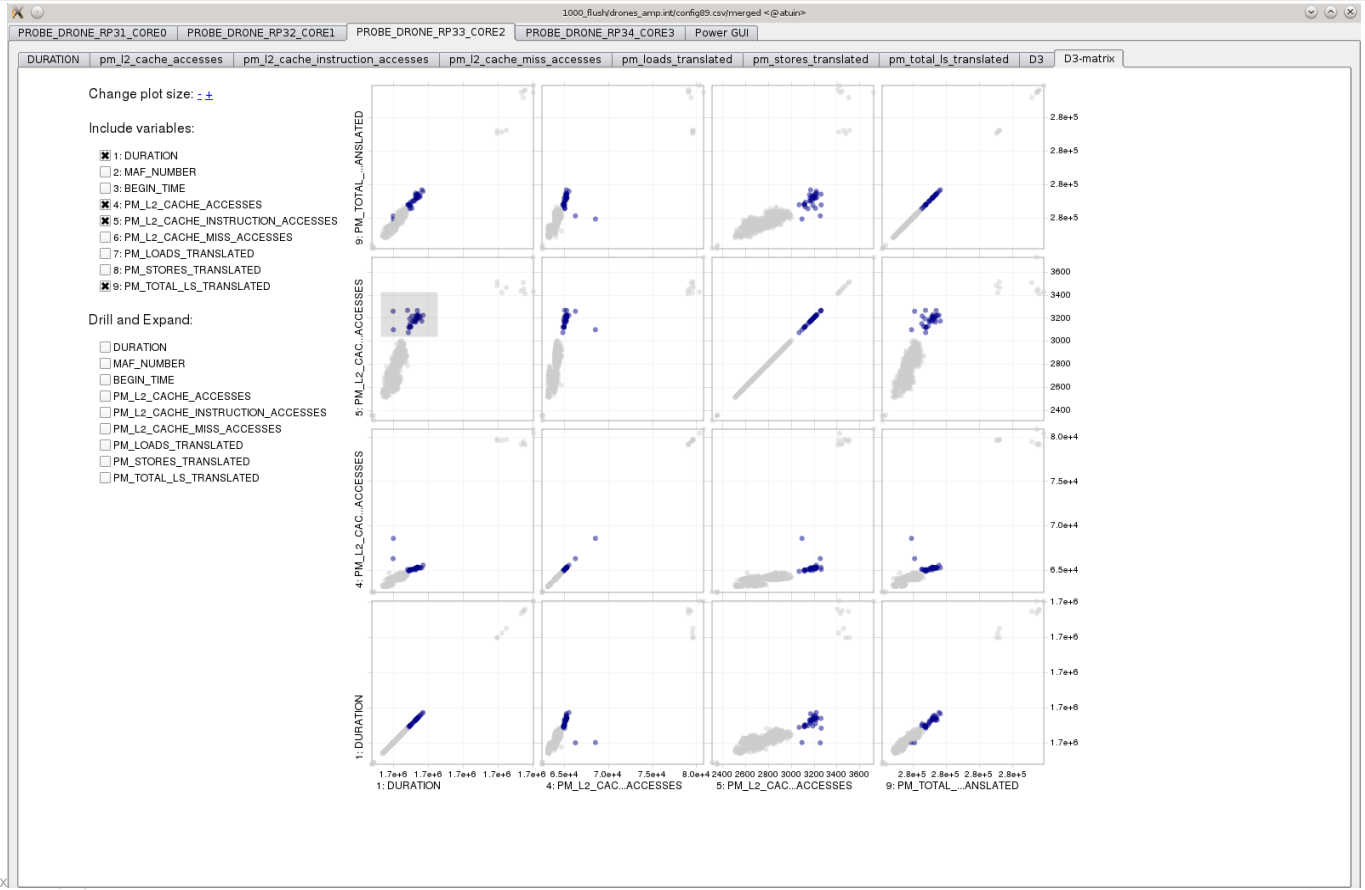


Access VS access correlograms



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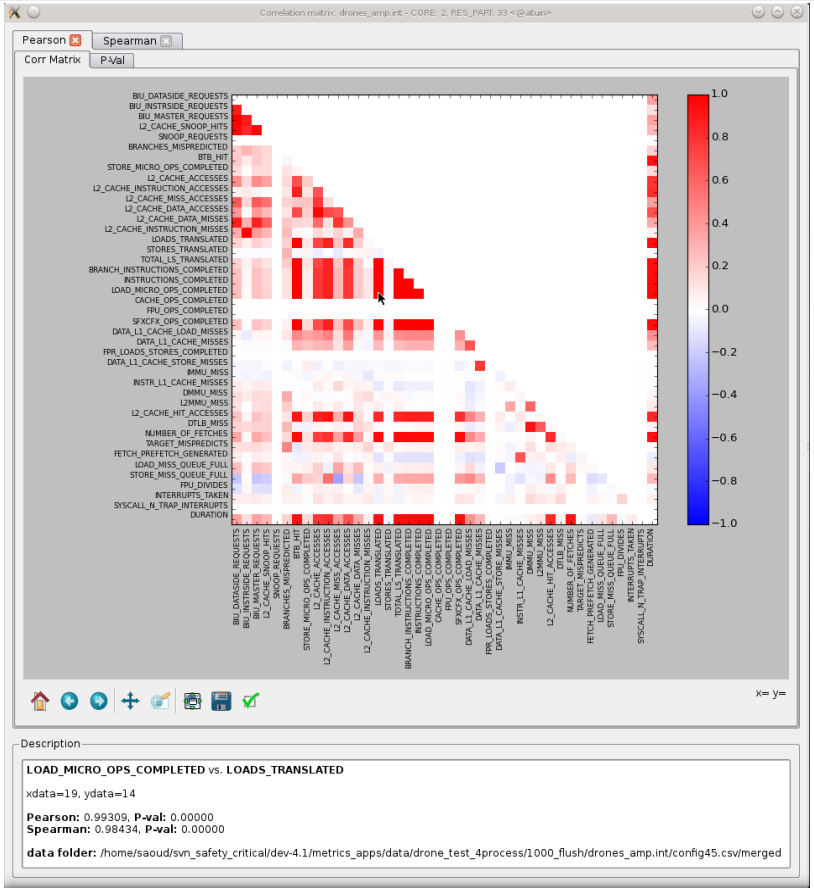
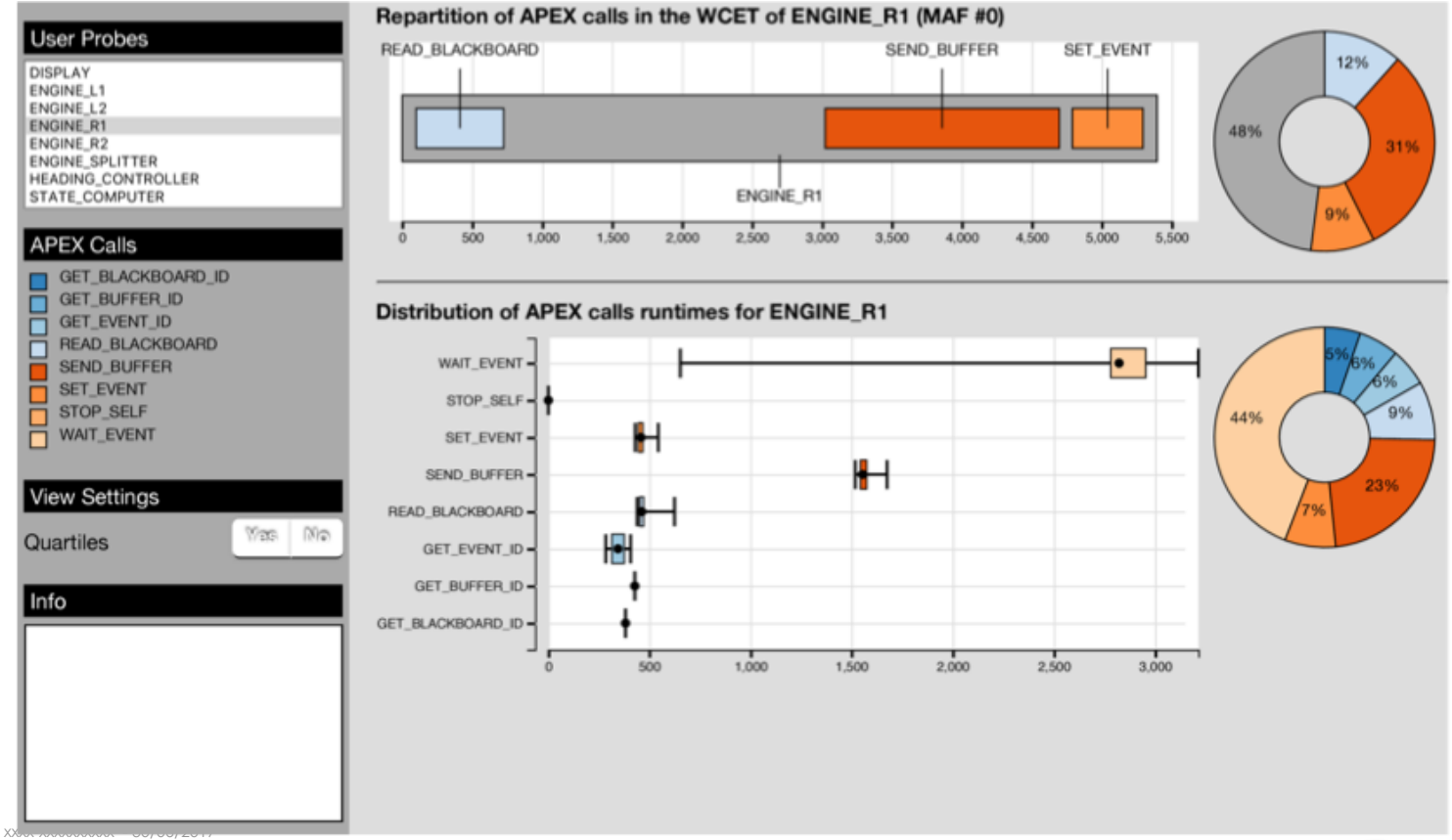
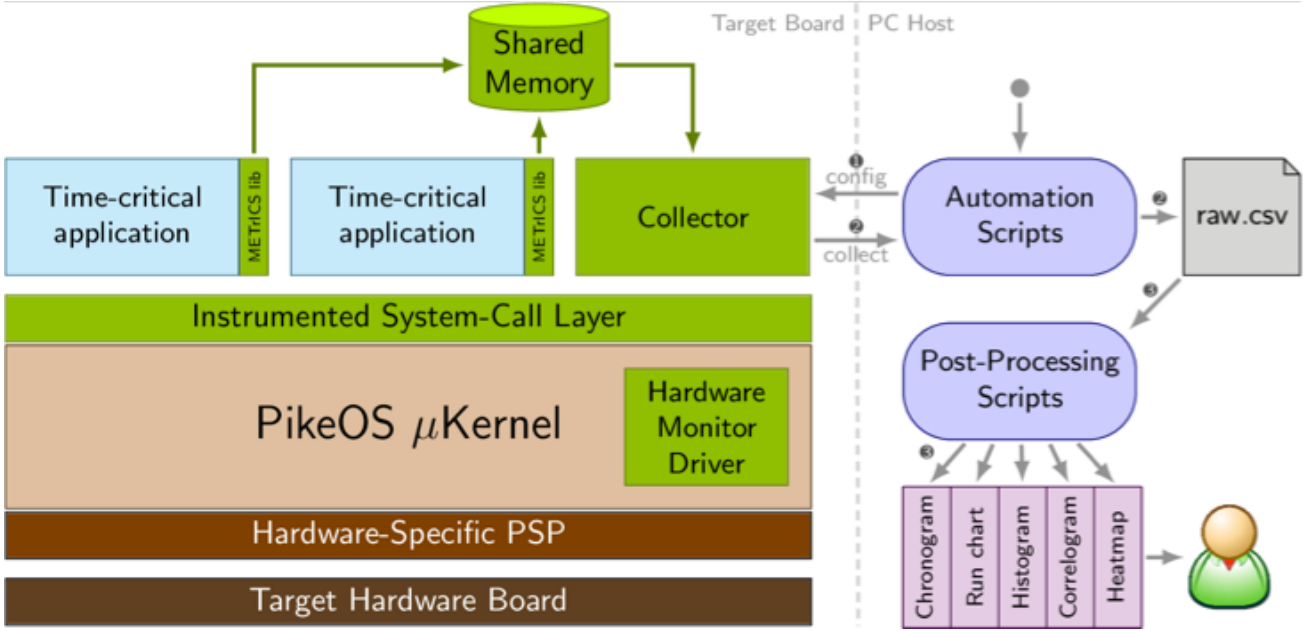


Rendering system call: repartition and distribution



METrICS: a Measurement Environment for Time Critical Systems



Measurement Environment

- Controlled accuracy and intrusiveness
- Can be turned into a RTE at the cost of more intrusiveness

Features

- Multiple hardware target
- Characterizing interference channels
- Visualization to guide expert's analysis

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